## CLAIMS

What is claimed is:

1. A digital circuit configured to locate and output a binary encoded position of a leading bit of a desired value in an input string of bits, comprising:

a plurality of input encoders, each accepting as input equal length sub-strings of the original input string, and each generating a binary encoded position of a leading bit of a desired value within the sub-string;

a plurality of bit value detectors, each also accepting as input the equal length sub-strings of the original input string, each detector indicating if the desired bit value exists within the sub-string;

an encoder arbitrator accepting as input the outputs of the bit value detectors and the binary encoded position from each of the input encoders, said arbitrator forwarding the binary encoded position of the leading bit of a desired value within the most significant sub-string; and

a most significant sub-string encoder that accepts as input the outputs from the bit value detectors, said sub-string encoder generating a binary encoded representation of the most significant sub-string comprising the desired bit value;

wherein the output of the encoder arbitrator and the output of the most significant sub-string encoder are concatenated to form the binary encoded representation of the position of the leading bit of a desired value in the input string of bits.

2. The digital circuit of claim 1 wherein the length of the input string is some multiple of two and the length of the binary encoded position is determined from the quotient log(input length)÷log(2).

3. The digital circuit of claim 2 wherein the length of the input string is 32 and the length of the binary encoded position is five.

4. The digital circuit of claim 3 wherein the sub-strings are eight bits long and the output from the input encoders and the output from the encoder arbitrators are each three bits long.

5. The digital circuit of claim 1 wherein:

the output of the encoder arbitrator represents the least significant portion and

the output of the most significant sub-string encoder represents the most significant portion of the binary encoded representation of the position of the leading bit of a desired value in the input string of bits.

6. The digital circuit of claim 5 wherein the encoder arbitrator further comprises identical sub-arbitrators for each output bit from the input encoders.

7. The digital circuit of claim 6 wherein the encoder sub-arbitrators further comprise:

a dynamic node to forward the bit signals received from each of the input encoders to the output of the sub-arbitrator; and

a plurality of switches controlled by the outputs from the bit value detectors, each switch capable of coupling the dynamic nodes to ground;

wherein if a bit value detector indicates that the desired bit value exists within the sub-string, the switches controlled by that bit value detector ground the signals on all less significant dynamic nodes.

8. A trailing bit detector configured to locate and output a binary encoded position of a trailing bit of a desired value in an input string of bits, comprising:

a plurality of input encoders, each accepting as input equal length sub-strings of the original input string, and each generating a binary encoded position of a trailing bit of a desired value within the sub-string;

a plurality of bit value detectors, each also accepting as input the equal length sub-strings of the original input string, each detector indicating if the desired bit value exists within the sub-string;

an encoder arbitrator accepting as input the outputs of the bit value detectors and the binary encoded position from each of the input encoders, said arbitrator forwarding the binary encoded position of the trailing bit of a desired value within the least significant sub-string; and

a least significant sub-string encoder accepting as input the outputs from the bit value detectors, said sub-string encoder generating a binary encoded representation of the least significant sub-string comprising the desired bit value;

wherein the output of the encoder arbitrator and the output of the least significant sub-string encoder are concatenated to form the binary encoded representation of the position of the trailing bit of a desired value in the input string of bits.

9. The digital circuit of claim 8 wherein the length of the input string is some multiple of two and the length of the binary encoded position is determined from the quotient log(input length)÷log(2).

10. The digital circuit of claim 9 wherein the length of the input string is 32 and the length of the binary encoded position is five.

11. The digital circuit of claim 10 wherein the sub-strings are eight bits long and the output from the input encoders and the output from the encoder arbitrators are each three bits long.

12. The digital circuit of claim 8 wherein:

the output of the encoder arbitrator represents the least significant portion and

the output of the least significant sub-string encoder represents the most significant portion of the binary encoded representation of the position of the trailing bit of a desired value in the input string of bits.

13. The digital circuit of claim 12 wherein the encoder arbitrator further comprises identical sub-arbitrators for each output bit from the input encoders.

14. The digital circuit of claim 13 wherein the encoder sub-arbitrators further comprise:

a dynamic node to forward the bit signals received from each of the input encoders to the output of the sub-arbitrator; and

a plurality of switches controlled by the outputs from the bit value detectors, each switch capable of coupling the dynamic nodes to ground;

wherein if a bit value detector indicates that the desired bit value exists within the sub-string, the switches controlled by that bit value detector ground the signals on all more significant dynamic nodes.

15. A method of locating and indicating the position of a leading binary bit value in a string of bits, comprising:

a) dividing the string of bits into shorter length segments, each segment represented by a unique binary value;

b) setting a bit flag for each of the shorter length segments that contain the bit value;

c) generating a binary location of the leading binary bit value for each of the shorter length segments;

d) selecting the unique binary value of the most significant shorter length segment that contains the bit value;

e) selecting the binary location generated in step c) for the most significant shorter length segment that contains the bit value; and

f) concatenating the unique binary value selected in step d) with the binary location selected in step e) to output a final binary representation of the location of the leading binary bit value in the original string of bits.

16. The method of claim 15, wherein selecting the binary location that is used in the final output further comprises:

receiving the binary locations from step c) and forwarding these binary location signals along dynamic nodes to the output;

using the bit flag signals to ground the dynamic nodes of all less significant segments if the bit flag indicates that a more significant segment contains the bit value.

17. The method of claim 16, wherein the shorter length segments are equal in length.

18. The method of claim 17, wherein the selection of the unique binary value in step d) and the selection of the binary location in step e) are executed in parallel.

19. The method of claim 18, wherein the unique binary value selected in step d) is the most significant portion of the final binary representation of the location of the leading binary bit value in the original string of bits.

20. A method of locating and indicating the position of a trailing binary bit value in a string of bits, comprising:

a) dividing the string of bits into shorter length segments, each segment represented by a unique binary value;

b) setting a bit flag for each of the shorter length segments that contain the bit value;

c) generating a binary location of the trailing binary bit value for each of the shorter length segments;

d) selecting the unique binary value of the least significant shorter length segment that contains the bit value;

e) selecting the binary location generated in step c) for the least significant shorter length segment that contains the bit value; and

f) concatenating the unique binary value selected in step d) with the binary location selected in step e) to output a final binary representation of the location of the trailing binary bit value in the original string of bits.

21. The method of claim 20, wherein selecting the binary location that is used in the final output further comprises:

receiving the binary locations from step c) and forwarding these binary location signals along dynamic nodes to the output;

using the bit flag signals to ground the dynamic nodes of all more significant segments if the bit flag indicates that a less significant segment contains the bit value.

22. The method of claim 21, wherein the shorter length segments are equal in length.

23. The method of claim 22, wherein the selection of the unique binary value in step d) and the selection of the binary location in step e) are executed in parallel.

24. The method of claim 23, wherein the unique binary value selected in step d) is the most significant portion of the final binary representation of the location of the trailing binary bit value in the original string of bits.

25. A method of locating and indicating the position of a leading binary bit value in an input string of bits, comprising:

sub-dividing the input string into substrings;

locating the position of the leading binary bit value in each substring and generating a first binary representation of this position for each substring;

identifying a most significant substring that includes the most significant bit value in the input string and generating a second binary representation of this substring; and

combining the first binary representation corresponding to the most significant substring and the second binary representation to form a single output binary representation of the position of a leading binary bit value in the input string.

26. The method of claim 25, wherein the substrings are equal length substrings.

27. The method of claim 26, further comprising:

assigning a bit flag to each substring; and

setting the bit flag if the substring includes the binary bit value.

28. The method of claim 27, further comprising:

using the bit flag to identify the substring that includes the most significant bit value in the input string; and

using the bit flag to select which of the first binary representations to combine with the second binary representation for the single output binary representation.

29. A method of locating and indicating the position of a trailing binary bit value in an input string of bits, comprising:

sub-dividing the input string into substrings;

locating the position of the trailing binary bit value in each substring and generating a first binary representation of this position for each substring;

identifying a least significant substring that includes the least significant bit value in the input string and generating a second binary representation of this substring; and

combining the first binary representation corresponding to the least significant substring and the second binary representation to form a single output binary representation of the position of a trailing binary bit value in the input string.

30. The method of claim 29, wherein the substrings are equal length substrings.

31. The method of claim 30, further comprising:

assigning a bit flag to each substring; and

setting the bit flag if the substring includes the binary bit value.

32. The method of claim 31, further comprising:

using the bit flag to identify the substring that includes the least significant bit value in the input string; and

using the bit flag to select which of the first binary representations to combine with the second binary representation for the single output binary representation.

33. A digital circuit for generating a binary encoded position of a leading bit value in an input string of bits, comprising:

a sub-dividing means for dividing the input string of bits into equal length sub-strings;

an input encoder means corresponding to each sub-string for generating a binary encoded position of a leading bit value in each sub-string;

a bit value detection means corresponding to each sub-string to indicate whether the bit value exists in each sub-string;

an output encoder means for selecting the most significant sub-string containing the bit value and generating a unique binary representation of this sub-string; and

an arbitrator means for selecting the most significant sub-string containing the bit value and forwarding the binary encoded position from the input encoder means corresponding to that sub-string;

wherein the output of the output encoder means and the output of the arbitrator means are combined to form a single binary representation of the position of the leading bit value in the input string of bits.

34. The digital circuit of claim 33 wherein:

the output of the arbitrator means represents the least significant portion and

the output of the output encoder means represents the most significant portion of the single binary representation of the position of the leading bit value in the input string of bits.

35. The digital circuit of claim 33 wherein the bit value detection means indicates whether the bit value exists in each sub-string by setting a bit corresponding to that sub-string.

36. The digital circuit of claim 33 wherein:

the output encoder means and the arbitrator means use the output from the bit value detection means to select the most significant sub-string containing the bit value.

37. The digital circuit of claim 36 wherein the arbitrator means further comprises identical sub-arbitrator means for each output bit from the input encoder means.

38. The digital circuit of claim 37 wherein the encoder sub-arbitrator means further comprise:

a dynamic node means to forward the bit signals received from each of the input encoder means to the output of the sub-arbitrator means; and

a plurality of switch means controlled by the outputs from the bit value detection means, each switch means capable of coupling the dynamic node means to ground;

wherein if any bit value detection means indicates that the bit value exists within that sub-string, the switch means controlled by that bit value detection means ground the signals on all less significant dynamic node means.

39. A digital circuit for generating a binary encoded position of a trailing bit value in an input string of bits, comprising:

a sub-dividing means for dividing the input string of bits into equal length sub-strings;

an input encoder means corresponding to each sub-string for generating a binary encoded position of a trailing bit value in each sub-string;

a bit value detection means corresponding to each sub-string to indicate whether the bit value exists in each sub-string;

an output encoder means for selecting the least significant sub-string containing the bit value and generating a unique binary representation of this sub-string; and

an arbitrator means for selecting the least significant sub-string containing the bit value and forwarding the binary encoded position from the input encoder means corresponding to that sub-string;

wherein the output of the output encoder means and the output of the arbitrator means are combined to form a single binary representation of the position of the trailing bit value in the input string of bits.

40. The digital circuit of claim 39 wherein:

the output of the arbitrator means represents the least significant portion and

the output of the output encoder means represents the most significant portion of the single binary representation of the position of the trailing bit value in the input string of bits.

41. The digital circuit of claim 39 wherein the bit value detection means indicates whether the bit value exists in each sub-string by setting a bit corresponding to that sub-string.

42. The digital circuit of claim 39 wherein:

the output encoder means and the arbitrator means use the output from the bit value detection means to select the least significant sub-string containing the bit value.

43. The digital circuit of claim 42 wherein the arbitrator means further comprises identical sub-arbitrator means for each output bit from the input encoder means.

44. The digital circuit of claim 43 wherein the encoder sub-arbitrator means further comprise:

a dynamic node means to forward the bit signals received from each of the input encoder means to the output of the sub-arbitrator means; and

a plurality of switch means controlled by the outputs from the bit value detection means, each switch means capable of coupling the dynamic node means to ground;

wherein if any bit value detection means indicates that the bit value exists within that sub-string, the switch means controlled by that bit value detection means ground the signals on all more significant dynamic node means.